DIGITAL LEVEL SHIFTER WITH REDUCED POWER DISSIPATION AND FALSE TRANSMISSION BLOCKING

ABSTRACT OF THE DISCLOSURE

A digital level shift circuit includes a level shifting device such as a high voltage MOS device and can also include feedback circuitry. The level shifting device is turned on to make an output transition, and the feedback circuitry obtains a feedback or acknowledge signal indicating that the transition was made. In response, the feedback circuitry turns off the level shifting device, which can reduce power dissipation. A digital level shift circuit that includes two n-channel devices and two p-channel devices can also include sense/prevent circuitry that senses when current greater than a threshold flows through both devices of one channel type and, in response, prevents output transitions from being made, which can avoid false transmissions due to rapid changes in offset voltage. Control circuitry in a digital level shift circuit can include both feedback circuitry and sense-prevent circuitry. In addition, the level shifting devices can be connected into a cross-acknowledge scheme in which none of the devices receives its acknowledge signal from the device to which it provides an acknowledge signal; this makes it possible to avoid a standoff between two devices. The control circuitry can also include, for each device, feedback detection circuitry to distinguish acknowledge signals, making it possible to restart a device that stops transmitting in response to a signal from another device that was not an acknowledge signal.